20th Euromicro Conference on Digital System Design

Vienna, Austria, Aug. 30th - Sept. 1st, 2017

Call for Papers

DSD 2017

Scope

The Euromicro Conference on Digital System Design (DSD) addresses all aspects of (embedded, pervasive and high-performance) digital and mixed HW/SW system engineering, covering the whole design trajectory from specification down to micro-architectures, digital circuits and VLSI implementations. It is a forum for researchers and engineers from academia and industry working on advanced investigations, developments and applications.

It focuses on today's and future challenges of advanced embedded, high-performance and cyber-physical applications; system and processor architectures for embedded and high-performance HW/SW systems; design methodology and design automation for all design levels of embedded, high-performance and cyber-physical systems; modern implementation technologies from full custom in nanometer technology nodes, through FPGAs, to MPSoC infrastructures.

Authors are kindly invited to submit their work according (but not limited) to the seven main topics of the conference main track. In addition, eight Special Sessions (with their own coordinators and subprogram committees) do also welcome contributions in specific themes of particular interest. All papers are reviewed following guidelines, quality requirements and thresholds that are common to all committees.

Main Topics

T1: Advanced applications of embedded and cyber-physical systems
T2: Application analysis and parallelization for embedded and high-performance design
T3: Specification, modeling, verification and test for systems, hardware and embedded software
T4: Design and synthesis of systems, hardware and embedded software
T5: Systems-on-a-chip and networks-on-a-chip
T6: Programmable/re-configurable/adaptable architectures
T7: New issues introduced by emerging technologies

Special Sessions/Organizers

DTFT: Dependability, Testing and Fault Tolerance in Digital Systems – *P. Fiser (CTU Prague, CZ), Z. Kotasek (TU Brno, CZ)*
MCSDIA: Mixed Criticality System Design, Implementation and Analysis – *K. Grüttner (OFFIS, DE), E. Villar (TEISA U Cantabria, ES)*
AHSA: Architectures and Hardware for Security Applications – *P. Kitsos (TEI of Western Greece, GR), R. S. Chakraborty (Indian Inst. of Tech. Kharagpur, IN)*
DCPS: Design of Cyber-Physical Systems – *M. Geilen, (TUE, NL), D. Quaglia (U Verona, IT)*
ASHWPA: Advanced Systems in Healthcare, Wellness and Personal Assistance – *F. Leporati (U Pavia, IT)*
ASAIT: Architectures and Systems for Automotive and Intelligent Transportation – *S. Niar (U Valenciennes, FR)*
SDIS: System Design for Intelligent Systems – *R. Jacobsen (Aarhus U, DK), E. Ebeid (U Southern Denmark, DK), B. Beach (U Southern Denmark, DK*
EPDSD: European Projects in Digital System Design – *F. Leporati (U Pavia, IT), L. Jozwiak (TUE, NL)*

Submission Guidelines

Authors are encouraged to submit their manuscripts to https://easychair.org/conferences/?conf=dsd2017. Should an unexpected web access problem be encountered, please contact the Program Chair by email (dsd2017@easychair.org).

Each manuscript should include the complete paper text, all illustrations, and references. The manuscript should conform to the IEEE format: single-spaced, double column, US letter page size, 10-point size Times Roman font, up to 8 pages. In order to conduct a blind review, no indication of the authors' names should appear in the manuscript, references included.

IEEE Conference Publishing Services (CPS) will publish accepted papers in the conference proceedings and the proceedings will be submitted to the IEEE Xplore Digital library and indexing services. Extended versions of selected best papers will be published in a special issue of the ISI indexed *"Microprocessors and Microsystems: Embedded Hardware Design"* Elsevier journal.

Important Dates

Deadline for paper submission: April 28th (Extended)
Notification of acceptance: June 10th
Camera ready papers: July 1st

More Information (web pages)

- **DSD 2017:** http://dsd-seaa2017.ocg.at
- **Euromicro:** www.euromicro.org

20th Euromicro Conference on Digital System Design

Vienna, Austria, Aug. 30th - Sept. 1st, 2017

Call for Papers

DSD 2017

Main Topics Description

T1: Advanced applications of embedded and cyber-physical systems
Challenging and highly-demanding modern applications in mobile systems; ubiquitous, wearable and implanted systems; (wireless) communication and networking; networked electronic media, multimedia and ambient intelligence; image and video processing; military, space, avionics, measurement, control and automotive applications; wireless sensor network applications; surveillance and security; environmental, agriculture, urban, building, transportation, traffic, energy, hazard and disaster monitoring and control.

T2: Application analysis and parallelization for embedded and high-performance hardware and software design
Application profiling, characterization and bottleneck detection; application restructuring for parallelism; application parallelization, information-flow analysis, scheduling and mapping for application-specific processors; MPSoC memory and communication architecture synthesis; HW/SW co-design and algorithm/architecture matching; combined hardware/software design space exploration and HW/SW system multi-objective optimization; parallelization, scheduling and mapping of applications for (heterogeneous) processor and MPSoC architectures; re-targetable (application-specific) compilation; architectural support for compilers/programming models; performance, energy consumption and other parametric analysis for HW/SW systems; analytical modeling and simulation tools; benchmark applications, workload and benchmarking for heterogeneous HW/SW systems; virtual and FPGA-based system prototyping.

T3: Specification, modeling, analysis, verification and test for systems, hardware and embedded software
Modeling, simulation, design and verification languages; functional, structural and parametric specification and modeling; model-based design and verification; system, hardware, and embedded software analysis, simulation, emulation, prototyping, formal verification, design-for-test and testing at all design levels; dependability, safety, security and fault-tolerance issues.

T4: Design and synthesis of systems, hardware and embedded software
Quality-driven design; model-, platform- and template-based design; design-space exploration; multi-objective optimization; system, processor, memory and communication architecture design; application scheduling and mapping to platforms; application-specific circuits and processors; arithmetic, signal, vector and graphics processing units; hardware accelerators; transaction level modeling and higher-level modeling; synthesis of asynchronous and dataflow systems; methods and CAD tools for analysis and synthesis of systems, architectures, embedded and high-performance software, and hardware at high-, logic- and physical level; methods and CAD tools for modeling, analysis and optimization of performance, energy consumption, reliability, robustness, safety, security, and testability.

T5: Systems-on-a-chip and networks-on-a-chip
(Heterogeneous) multiprocessor systems on-a-chip (MPSoC), hardware multiprocessors and complex accelerators; generic system platforms and platform-based design; processor, memory and communication architectures; 3D MPSoCs and 3D NoCs; ASIP- and GPU-based platforms; software design and programming models for multicore platforms; IP design, standardization and reuse; parallelism exploitation and scalability techniques; virtual components; system of systems; compiler assisted MPSoCs; hardware support for embedded kernels; embedded software features; static, run-time and dynamic optimizations of embedded MPSoCs; benchmarks and benchmarking for MPSoCs; NoC architecture and quality of service; power dissipation and energy issues in SoCs and NoCs.

T6: Programmable/reconfigurable/adaptable architectures
Design methodologies and tools for reconfigurable computing; run-time, partial and dynamic reconfiguration; fine-grained, mixed-grained and coarse-grained reconfigurable architectures; reconfigurable interconnections and NoCs; FPGAs; systems on reconfigurable chip; system FPGAs, structured ASICs; co-processors; processing arrays; programmable fabrics; adaptive computing devices, systems and software; adaptable ASIPs and ASIP-based MPSoCs; hardware accelerators; optimization of FPGA-based cores; shared resource management; novel models, design algorithms and tools for FPGAs and FPGA-based systems; rapid prototyping systems and platforms; adaptable wireless and mobile systems.

T7: New issues introduced by emerging technologies
Important issues for system, circuit and embedded software design introduced by e.g. the nanometer CMOS and beyond CMOS technologies, 3D integration, optical and other new memory and communication technologies; new human-machine interfaces; neural- and bio-computation; (bio)sensor and sensor network technologies; pervasive and ubiquitous computing (Internet of Things); related design methods and EDA tools; Flexible Digital Radio-digital architecture design and methodologies concepts for multi-standard, multi-mode flexible radios.

Special Sessions

In addition to the above Main Topics (the Conference "traditional core"), papers are also sought for special sessions. Prospective authors are invited to submit papers related to: system and SoC dependability and testing (DTFT); integration of multiple functions with different criticality and certification assurance levels (MCSDIA); architectures and hardware for secure embedded systems, e.g. smart cards, DSPs, RFID and Wireless Sensor Networks (AHSA); heterogeneous distributed pervasive networked embedded and cyber-physical systems (DCPS); advanced systems for improving quality of life, healthcare and personal assistance (ASHWPA); new architectures and systems for automotive and intelligent transportation (ASAIT); design of digital systems for next-generation power grids (SDSG); or issues and solutions researched in starting, ongoing or recently finished European Projects in the (embedded, pervasive and high-performance) Digital System Design Area (EPDSD).